**REMARKS**

Claims 1-44 are pending in the present application.

Claims 1-44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rowlands et al. (U.S. Patent Application Publication No. 2004/0034747) (hereinafter "Rowlands1"), in view of Rowlands et al. (U.S. Patent Application Publication No. 2003/0217216 now U.S. Patent No. 6,948,035) (hereinafter "Rowlands2"), and in further view of Singhal et al. (U.S. Patent No. 5,978,874). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part

> wherein in response to receiving ***from the additional node*** via the inter-node network, a coherency message requesting an access right to a coherency unit, the interface is configured to send *a first type of address packet* **on the address network** if a global access state of the coherency unit *in the node* is a modified state and *to send a second type of address packet* **on the address networ**k if the global access state of the coherency unit *in the node* is *not* the modified state; and
>
> wherein if the given active device has an ownership responsibility for the coherency unit, the given active device is configured to ignore the second type of address packet and to respond to the first type of address packet." (Emphasis added)

The Examiner asserts Rowlands1 teaches "in response to receiving *from the additional node* via the inter-node network, a coherency message requesting an access right to a coherency unit, the interface is configured to send *a first type of address packet* on the address network if a global access state of the coherency unit *in the node* is a modified state and *to send a second type of address packet* on the address network if the global access state of the coherency unit *in the node* is *not* the modified state" at paragraphs [0072]-[0074]. The Examiner further asserts "NC1118 is responsible for implementing the inter-node coherency using RLD 1116" and "if the line is shared (i.e., not modified) a Kill command can be issued. If the line is modified, a cFlush command must be issued."

However, Applicant submits Rowlands1 actually discloses

> Finally, the coherent state of the cache line must be tracked. The RLD 1116 contains this information. The RLD 1116 acts very similarly to a cache tag array. When an access ***on the MP bus 1114*** occurs to that line, it checks the RLD 1116 to see if the line is present, and if it is, what action needs to be taken. (*See* paragraph [0073]) (Emphasis added)
>
> If an RLD 1116 entry needs to be allocated, but the RLD is full, an entry needs to be cleared out of the RLD. This behaves like a cache evict, except the data is remote. To complete the evict, the data needs to be retrieved/invalidated. This evict can be done by issuing a probe to the agent(s) borrowing the line. If the line is Shared, a Kill command can be issued. If it is borrowed Modified, a cFlush must be issued. (*See* paragraph [0074]) (Emphasis added)

From the foregoing disclosure, Applicant submits Rowlands1 is disclosing the NC1118 receiving a request on the MP bus, which is the internal inter-processor bus, and *NOT* from the external network, as recited in claim 1. Furthermore, the issuance of either a Kill command or the cFlush command is in response to receiving the probe results of a probe sent by the NC1118 because an entry in the RLD needs to be cleared. This is clearly different than "**in response to receiving *from the additional node***" "a coherency message *requesting an access right* to a coherency unit," sending "*a first type of address packet* on the address network if a global access state of the coherency unit *in the node* is a modified state" and sending "*a second type of address packet* on the address network if the global access state of the coherency unit *in the node* is *not* the modified state."

Accordingly, Applicant submits Rowlands1 does not teach the above limitation recited in claim 1, as suggested by the Examiner.

The Examiner acknowledges that Rowlands1 does not teach "wherein if the given active device has an ownership responsibility for the coherency unit, the given active device is configured to ignore the second type of address packet and to respond to the first type of address packet." However, the Examiner seems to assert that the combination of Rowlands 1, Rowlands2 and Singhal teaches the limitation, since the Examiner recites several passages from each reference to apparently illustrate how cache

lines may be borrowed and in what states and by which agents. The Examiner then asserts that because Rowlands2 discloses "that a single transaction may be used for probes and in still other embodiments, there may be a probe generated transaction that invalidates agent copies of the cache block and another probe generated transaction that permits agents to retain shared copies of the cache block (Rowlands 2, par. [0058])," that this somehow teaches the first type of address packet and the second type of address packet. Applicant respectfully disagrees.

More particularly, Applicant submits the combination as suggested by the Examiner seems to disclose various global access states and whether an agent can be an owner and not have the data, etc. The Examiner argues at length about how an agent can have ownership but not the data. The Examiner then makes an assumption that this somehow suggests that because a node has ownership but does not have the data, it ignores a request for the data. Applicant submits this is just not true and is purely speculation by the Examiner.

The Examiner further cites Rowlands1 at paragraph [0071], however, Rowlands1 merely discloses that "if the line is borrowed in the Modified state, that borrowing node has ownership. It can share the line among the agents in that processing node, or it can give an exclusive ownership to a single agent, so that it can be modified intranode." However, this is in reference to paragraph [0070] which discusses that a cache line may be borrowed by a remote node in either a modified state or a shared state, which still does not teach the limitations in Applicant's claims. Applicant believes the Examiner is making the above assumptions regarding the cited references by using improper hindsight obtained SOLELY from Applicant's claimed invention.

In addition, Applicant has attempted to piece together the various phrases cited by the Examiner. However, Applicant continues to assert that the combination does not teach each and every limitation. More particularly, Applicant submits although the combination of the cited references teaches various coherency protocols and ways of handling local and remote transactions, as described above, none of the references taken

either singly or in combination, teaches or suggests the combination of features recited in claim 1. Accordingly Applicant submits the Examiner has not established a *prima facie* case of obviousness.

Thus, Applicant submits claim 1 along with its dependent claims, patentably distinguishes over the cited references for the reasons given above.

Applicant's claims 15, 31, and 44 include features that are similar to the features recited in claim 1. Thus, Applicant submits claims 15, 31, and 44 along with their respective dependent claims, patentably distinguish over the cited references for at least the reasons given above.

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-95101/SJC.

Respectfully submitted,

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